

What is claimed is:

1 1. A processor which decodes and executes an instruction
2 sequence, the processor comprising:

3 a state hold means for holding, when a predetermined
4 instruction is executed, a renewal state for an execution
5 result of the predetermined instruction;

6 an obtaining means for obtaining an instruction
7 sequence composed of instructions matching instructions
8 assigned to an instruction set of the processor,

9 wherein the instruction set is assigned first
10 conditional instructions, a first state condition for a
11 first conditional instruction being mutually exclusive
12 with a second state condition for a second conditional
13 instruction which has a same operation code as the first
14 conditional instruction, the instruction set not being
15 assigned the second conditional instruction, and the first
16 state condition and the second state condition specifying
17 either of one state and a plurality of states;

18 a decoding means for decoding each instruction in the
19 obtained instruction sequence one by one;

20 a judging means for judging whether the renewal state
21 is included in either of the state and the plurality of
22 states specified by the first state condition in the first
23 conditional instruction, when the decoding means decodes

24 the first conditional instruction; and
25 an execution means for executing, only if a judgement
26 result by the judging means is affirmative, an operation
27 specified by the operation code in the first conditional
28 instruction decoded by the decoding means.

1 2. The processor of Claim 1,
2 wherein the renewal state shows a relation between
3 magnitudes of two comparison objects a and b, the relation
4 corresponding to an execution result of a type of
5 comparison instruction,

6 wherein execution of a first conditional instruction
7 is only possible after a comparison instruction, and the
8 instruction set is assigned three types of first
9 conditional instructions, the first condition states of
10 the three types of first conditional instructions being:

- 11 1. one out of "a=b" and "a≠b";
- 12 2. one out of "a≥b" and "a<b"; and
- 13 3. one out of "a≤b" and "a>b".

1 3. The processor of Claim 2,
2 wherein an operation code included in a conditional
3 instruction is one of a transfer operation code, an
4 arithmetic operation code, and a logic operation code.

1 4. A processor which decodes and executes an instruction
2 sequence, the processor including:

3 an obtaining means for obtaining an instruction
4 sequence composed of instructions matching instructions
5 assigned to an instruction set of the processor,

6 wherein the instruction set is assigned at least one
7 first conditional flag setting instruction, at least one
8 second conditional flag setting instruction, and at least
9 one conditional execution instruction,

10 each first conditional flag setting instruction
11 including a first condition, and each second conditional
12 flag setting instruction including a second condition,
13 each first condition being mutually exclusive with one of
14 the second conditions,

15 each conditional execution instruction including an
16 operation code that is not included in any other
17 conditional execution instruction in the instruction
18 set;

19 a decoding means for decoding each instruction in the
20 obtained instruction sequence one by one;

21 a conditional flag for holding a judgement result as
22 to whether a predetermined condition is satisfied;

23 a judging means for judging, when the decoding means
24 decodes the first conditional flag setting instruction,
25 whether the first condition in the first conditional flag

26 setting instruction is satisfied and has the conditional
27 flag hold a judgement result for the first condition and,
28 when the decoding means decodes the second conditional
29 flag setting instruction, judges whether the second
30 condition in the second conditional flag setting
31 instruction is satisfied and has the conditional flag hold
32 a judgement result for the second condition; and

33 an execution means for executing, only if the
34 decoding means decodes the conditional execution
35 instruction and the judgement result held by the
36 conditional flag indicates that a condition for the
37 conditional execution instruction is satisfied, an
38 operation specified by the operation code in the
39 conditional execution instruction.

1 5. The processor of Claim 4,
2 wherein each of the first conditional flag setting
3 instruction and the second conditional flag setting
4 instruction specifies two comparison objects a and b,
5 wherein the instruction set is assigned three types
6 of first conditional flag setting instructions and three
7 types of second conditional flag setting instructions, the
8 first conditions of the first conditional flag setting
9 instructions being a combination of the following
10 conditions:

11 1. one out of "a=b" and "a≠b";
12 2. one out of "a≥b" and "a<b"; and
13 3. one out of "a≤b" and "a>b",
14 the second conditions of the second conditional
15 instructions being three mutually exclusive conditions for
16 the three first conditions.

1 6. The processor of Claim 5,
2 wherein the instruction set is further assigned two
3 types of first conditional flag setting instructions and
4 two types of second conditional flag setting
5 instructions,

6 the first conditions of the first conditional flag
7 setting instructions being a combination of the following
8 conditions:

9 4. one out of "a≥b" and "a<b"; and
10 5. one out of "a≤b" and "a>b"
11 (where a and b of conditions 4 and 5 are compared with
12 signs of a and b being taken into account),
13 and the second conditions of the second conditional
14 flag setting instructions being mutually exclusive with
15 the first conditions.

1 7. The processor of Claim 5,
2 wherein an operation code included in a conditional

3 execution instruction is one of a transfer operation code,
4 an arithmetic operation code, a logic operation code, and
5 a branch operation code.

1 8. An instruction conversion apparatus for converting
2 instruction sequences not including conditional
3 instructions into instruction sequences including
4 conditional instructions, each of the conditional
5 instructions including a condition and an operation code
6 and having a processor execute an operation specified by
7 the operation code only if the condition is satisfied, the
8 apparatus comprising:

9 an obtaining means for obtaining an instruction
10 sequence which does not include conditional
11 instructions;

12 an instruction sequence detection means for
13 detecting, out of the obtained instruction sequence, a
14 conversion target instruction sequence which transfers
15 different transfer objects to a same storage resource
16 depending on whether a predetermined condition is
17 satisfied;

18 a judging means for judging whether an instruction
19 set of a specialized processor is assigned a conditional
20 instruction including a same condition as the
21 predetermined condition; and

22 a conversion means for converting, when a judgement
23 result by the judging means is affirmative, the conversion
24 target instruction sequence into an instruction sequence
25 including a conditional instruction including the
26 predetermined condition and for interchanging, when the
27 judgement result by the judging means is negative, the
28 transfer objects of the conversion target instruction
29 sequence and converts the conversion target instruction
30 sequence into an instruction sequence including a
31 conditional instruction including a condition that is
32 mutually exclusive with the predetermined condition.

1 9. The apparatus of Claim 8,

2 wherein the instruction set of the specialized
3 processor is assigned a conditional instruction including
4 a condition that is mutually exclusive with a condition
5 included in a conditional instruction judged as not
6 assigned to the instruction set by the judging means,
7 and

8 conditions included in conditional instructions for
9 a same operation assigned to the instruction set are not
10 mutually exclusive.

1 10. The apparatus of Claim 9,

2 wherein execution of a conditional instruction is

3 only possible after a comparison instruction, and
4 the instruction set is assigned three types of
5 conditional instructions for each operation according to
6 a relation between magnitudes of two comparison objects
7 compared by the comparison instruction, the conditions of
8 the three types of conditional instructions being:

- 9 1. one out of "a=b" and "a≠b";
- 10 2. one out of "a≥b" and "a<b"; and
- 11 3. one out of "a≤b" and "a>b".

1 11. The apparatus of Claim 10,

2 wherein each of the transfer objects is one of a
3 numerical value, a value indicated by a different storage
4 resource, an operation result of a numerical value and a
5 value indicated by the different storage resource, an
6 operation result of numerical values, and an operation
7 result of values indicated by the different storage
8 resource.

1 12. The apparatus of Claim 11,

2 wherein the conversion target instruction sequence
3 consecutively includes a conditional branch instruction
4 for branching to a next instruction but two, a transfer
5 instruction for transferring a transfer object to a
6 storage resource, an unconditional branch instruction for

7 branching to a next instruction but one, and a transfer
8 instruction for transferring another transfer object to
9 the storage resource.

1 13. An instruction conversion apparatus for converting
2 conditional instructions included in instruction
3 sequences, each of the conditional instructions including
4 a condition and an operation code and having a processor
5 execute an operation specified by the operation code only
6 if the condition is satisfied, the apparatus comprising:

7 an obtaining means for obtaining an instruction
8 sequence including conditional instructions;

9 a conditional instruction detection means for
10 detecting a conditional instruction included in the
11 obtained instruction sequence;

12 a first judging means for judging whether the
13 detected conditional instruction is assigned to an
14 instruction set of a specialized processor;

15 a second judging means for judging, when a judgement
16 result by the first judging means is negative, whether the
17 obtained instruction sequence includes a conversion target
18 instruction sequence which transfers different transfer
19 objects to a same storage resource depending on whether a
20 predetermined condition of the detected conditional
21 instruction is satisfied; and

22 a conversion means for interchanging, when a
23 judgement result by the second judging means is
24 affirmative, the transfer objects and converts the
25 detected conditional instruction into a conditional
26 instruction including a condition that is mutually
27 exclusive with the predetermined condition.

1 14. The apparatus of Claim 13,
2 wherein the instruction set of the specialized
3 processor is assigned a conditional instruction including
4 a condition being mutually exclusive with a condition
5 included in a conditional instruction judged as not
6 assigned to the instruction set by the first judging
7 means, and

8 conditions included in conditional instructions for
9 a same operation assigned to the instruction set are not
10 mutually exclusive.

1 15. The apparatus of Claim 14,
2 wherein execution of a conditional instruction is
3 only possible after a comparison instruction, and
4 the instruction set is assigned three types of
5 conditional instructions for each operation according to
6 a relation between magnitudes of two comparison objects
7 compared by the comparison instruction, the conditions of

8 the three types of conditional instructions being:

- 9 1. one out of "a=b" and "a≠b";
10 2. one out of "a≥b" and "a<b"; and
11 3. one out of "a≤b" and "a>b".

1 16. The apparatus of Claim 15,

2 wherein each of the transfer objects is one of a
3 numerical value, a value indicated by a different storage
4 resource, an operation result of a numerical value and a
5 value indicated by the different storage resource, an
6 operation result of numerical values, and an operation
7 result of values indicated by the different storage
8 resource.

1 17. The apparatus of Claim 16,

2 wherein the conversion target instruction sequence
3 consecutively includes a comparison instruction for
4 comparing two comparison objects, a transfer instruction
5 for transferring a predetermined transfer object to a
6 predetermined storage resource, and a conditional
7 instruction for transferring a transfer object that
8 differs from the predetermined transfer object to the
9 predetermined storage resource only if a predetermined
10 condition is satisfied.

- 1 18. The apparatus of Claim 13,
2 wherein the conversion means includes:
3 an inverse conversion means for converting, when a
4 judgement result by the second judging means is negative,
5 the instruction sequence including the detected
6 conditional instruction into an instruction sequence not
7 including the detected conditional instruction.
- 1 19. An instruction conversion apparatus for converting an
2 instruction sequence not including a conditional flag
3 setting instruction and a conditional execution
4 instruction into an instruction sequence including a
5 conditional flag setting instruction and a conditional
6 execution instruction,
7 each conditional flag setting instruction including
8 a condition, having a specialized processor judge whether
9 the condition is satisfied, and having a conditional flag
10 hold a judgement result as to whether the condition is
11 satisfied,
12 each conditional execution instruction including an
13 operation code and having the specialized processor
14 execute an operation specified by the operation code only
15 if a condition of the conditional execution instruction is
16 satisfied,
17 the apparatus comprising:

18 an obtaining means for obtaining an instruction
19 sequence which does not include conditional flag setting
20 instructions and conditional execution instructions;

21 an instruction sequence detection means for
22 detecting, out of the obtained instruction sequence, a
23 conversion target instruction sequence which transfers
24 different transfer objects to a same storage resource
25 depending on whether a predetermined condition is
26 satisfied; and

27 a conversion means for converting the conversion
28 target instruction sequence into an instruction sequence
29 which includes a conditional flag setting instruction
30 including the predetermined condition and a conditional
31 execution instruction including an operation code which
32 specifies an operation for transferring a transfer object
33 to the storage resource when the predetermined condition
34 is satisfied.

1 20. The apparatus of Claim 19,

2 wherein a condition of a conditional flag setting
3 instruction which is convertible by the conversion means
4 is mutually exclusive with a condition of another
5 conditional flag setting instruction which is convertible
6 by the conversion means.

1 21. The apparatus of Claim 20,
2 wherein each conditional flag setting instruction
3 specifies two comparison objects a and b,
4 wherein the instruction set is assigned three types
5 of first conditional flag setting instructions and three
6 types of second conditional flag setting instructions, the
7 first conditions of the first conditional flag setting
8 instructions being a combination of the following
9 conditions:
10 1. one out of "a=b" and "a≠b";
11 2. one out of "a≥b" and "a<b"; and
12 3. one out of "a≤b" and "a>b",
13 the second conditions of the second conditional flag
14 setting instructions being three mutually exclusive
15 conditions for the three first conditions.

1 22. The apparatus of Claim 21,
2 wherein each of the transfer objects is one of a
3 numerical value, a value indicated by a different storage
4 resource, an operation result of a numerical value and a
5 value indicated by the different storage resource, an
6 operation result of numerical values, and an operation
7 result of values indicated by the different storage
8 resource.

1 23. The apparatus of Claim 22,
2 wherein the conversion target instruction sequence
3 consecutively includes a comparison instruction for
4 comparing two comparison objects, a conditional branch
5 instruction for branching to a next instruction but two
6 when a predetermined condition is satisfied, a transfer
7 instruction for transferring a predetermined transfer
8 object to a predetermined storage resource, an
9 unconditional branch instruction for branching to a next
10 instruction but one, and a transfer instruction for
11 transferring a transfer object that differs from the
12 predetermined transfer object to the predetermined storage
13 resource.

1 24. The apparatus of Claim 22,
2 wherein the conversion target instruction sequence
3 consecutively includes a comparison instruction for
4 comparing two comparison objects, a transfer instruction
5 for transferring a predetermined transfer object to a
6 predetermined storage resource, and a conditional
7 instruction for transferring a transfer object that
8 differs from the predetermined transfer object to the
9 predetermined storage resource only if a predetermined
10 condition is satisfied.

1 25. The apparatus of Claim 22,
2 wherein the conversion target instruction sequence
3 consecutively includes a comparison instruction for
4 comparing two comparison objects, a conditional
5 instruction for transferring a predetermined transfer
6 object to a predetermined storage resource only if a
7 predetermined condition is not satisfied, and a
8 conditional instruction for transferring a transfer object
9 that differs from the predetermined transfer object to the
10 predetermined storage resource only if the predetermined
11 condition is satisfied.

1 26. A computer-readable recording medium which records an
2 instruction conversion program for having a computer
3 perform a method of converting instruction sequences not
4 including conditional instructions into instruction
5 sequences including conditional instructions, each of the
6 conditional instructions including a condition and an
7 operation code and having a processor execute an operation
8 specified by the operation code only if the condition is
9 satisfied, the program comprising:

10 an obtaining step for obtaining an instruction
11 sequence which does not include conditional
12 instructions;
13 an instruction sequence detection step for detecting,

14 out of the obtained instruction sequence, a conversion
15 target instruction sequence which transfers different
16 transfer objects to a same storage resource depending on
17 whether a predetermined condition is satisfied;

18 a judging step for judging whether an instruction set
19 of a specialized processor is assigned a conditional
20 instruction including a same condition as the
21 predetermined condition; and

22 a conversion step for converting, when a judgement
23 result in the judging step is affirmative, the conversion
24 target instruction sequence into an instruction sequence
25 including a conditional instruction including the
26 predetermined condition and for interchanging, when the
27 judgement result in the judging step is negative, the
28 transfer objects of the conversion target instruction
29 sequence and converts the conversion target instruction
30 sequence into an instruction sequence including a
31 conditional instruction including a condition that is
32 mutually exclusive with the predetermined condition.

1 27. A computer-readable recording medium which records an
2 instruction conversion program for having a computer
3 perform a method of converting conditional instructions
4 included in instruction sequences, each of the conditional
5 instructions including a condition and an operation code

6 and having a processor execute an operation specified by
7 the operation code only if the condition is satisfied, the
8 program comprising:

9 an obtaining step for obtaining an instruction
10 sequence including conditional instructions;

11 a conditional instruction detection step for
12 detecting a conditional instruction included in the
13 obtained instruction sequence;

14 a first judging step for judging whether the detected
15 conditional instruction is assigned to an instruction set
16 of a specialized processor;

17 a second judging step for judging, when a judgement
18 result in the first judging step is negative, whether the
19 obtained instruction sequence includes a conversion target
20 instruction sequence which transfers different transfer
21 objects to a same storage resource depending on whether a
22 predetermined condition of the detected conditional
23 instruction is satisfied; and

24 a conversion step for interchanging, when a judgement
25 result in the second judging step is affirmative, the
26 transfer objects and converts the detected conditional
27 instruction into a conditional instruction including a
28 condition that is mutually exclusive with the
29 predetermined condition.

1 28. A computer-readable recording medium which records an
2 instruction conversion program for having a computer
3 perform a method of converting an instruction sequence not
4 including a conditional flag setting instruction and a
5 conditional execution instruction into an instruction
6 sequence including a conditional flag setting instruction
7 and a conditional execution instruction,

8 each conditional flag setting instruction including
9 a condition, having a specialized processor judge whether
10 the condition is satisfied, and having a conditional flag
11 hold a judgement result as to whether the condition is
12 satisfied,

13 each conditional execution instruction including an
14 operation code and having the specialized processor
15 execute an operation specified by the operation code only
16 if a condition of the conditional execution instruction is
17 satisfied,

18 the program comprising:

19 an obtaining step for obtaining an instruction
20 sequence which does not include conditional flag setting
21 instructions and conditional execution instructions;

22 an instruction sequence detection step for detecting,
23 out of the obtained instruction sequence, a conversion
24 target instruction sequence which transfers different
25 transfer objects to a same storage resource depending on

26 whether a predetermined condition is satisfied; and
27 a conversion step for converting the conversion
28 target instruction sequence into an instruction sequence
29 which includes a conditional flag setting instruction
30 including the predetermined condition and a conditional
31 execution instruction including an operation code which
32 specifies an operation for transferring a transfer object
33 to the storage resource when the predetermined condition
34 is satisfied.